

## CLAIMS:

1. A data processing circuit for processing an input data pattern and for outputting an output data pattern after a processing delay which depends on a processing activity of said data processing circuitry, said data processing circuitry comprising:

a) estimation means for estimating said processing delay based on said input data pattern;

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b) control means for controlling said processing by said data processing circuit in response to said estimated processing delay.

2. A circuitry according to claim 1, wherein said estimation means comprises a

10 look-up table for storing said estimated processing delay.

3. A circuitry according to claim 2, wherein said look-up table is addressed by said input data pattern to output said estimated processing delay.

15 4. A circuitry according to any one of the preceding claims, wherein said estimation means comprises a programmable delay line which is programmed by said input data pattern.

5. A circuitry according to claim 4, wherein said programmable delay line is  
20 adapted to generate an output signal after expiry of said estimated processing delay.

6. A circuitry according to any one of the preceding claims, wherein said estimation means is adapted to estimate said processing delay based on a sequence of input data patterns.

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7. A circuitry according to any one of the preceding claims, wherein said control means is arranged to derive said processing activity from said estimated delay, and to control power supply of said data processing circuitry in response to said derived processing activity.

8. A circuitry according to any one of claims 1 to 6, wherein said control means is adapted to control the clock supply to said data processing circuitry in response to said estimated processing delay.

5 9. A circuitry according to claim 8, wherein said data processing circuitry has a pipeline structure and said control means is adapted to selectively gate said clock supply for each stage of said pipeline structure.

10 10. A circuitry according to claim 9, wherein said control means is arranged to un-gate said clock supply if the previous stage has produced a valid output signal and the following stage has stored said output signal.

11. A circuitry according to any one of the preceding claims, wherein said estimated processing delay is expressed as a number of cycles of said clock signal.

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12. A method of controlling processing of an input data pattern, wherein a predetermined output data pattern is generated after a processing delay which depends on an activity of said processing, said method comprising the steps of:

- 20 a) estimating said processing delay based on said input data pattern; and  
b) performing said processing control in response to said estimated processing delay.

13. A method according to claim 12, wherein said processing control is a power control based on an activity monitoring.

25 14. A method according to claim 12, wherein said processing control is a control of a clock supply to a synchronous pipeline structure.